ABSTRACT OF THE DISCLOSURE

A system and method for maintaining a stable synchronization state in a programmable clock synchronizer for effectuating data transfer between first circuitry disposed in a first clock domain and second circuitry disposed in a second clock domain. In a system embodiment, a first circuit portion generates a load signal indicative of a known acceptable state for which a cycle can be loaded. A second circuit portion is in communication with the first circuit portion in order to generate a lock signal indicative of a tolerable tracked skew between a first clock signal of the first clock domain and a second clock signal of the second clock domain. A third circuit portion, responsive to the load signal, the lock signal and a zero skew point indicator, generates a synchronization stable state signal indicative of locking between the first clock signal and the second clock signal.